AMENDMENTS TO THE CLAIMS

Claims 1-13 (Cancelled.)

14. (Currently Amended) A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a top surface;

etching the layer of insulation material to form a plurality of first trenches in the layer of insulation material, ~~the trenches~~ each first trench having a first bottom surface vertically spaced a first distance apart from the top surface; and

etching the layer of insulation material and the plurality of first trenches to form a second trench in the layer of insulation material, the second trench having ~~the~~ a plurality of ~~first trenches, the first trenches having a~~ second bottom ~~surface~~ surfaces vertically spaced a second distance apart from the top surface, ~~the second distance being greater than the first distance;~~ and third bottom surfaces vertically spaced a third distance apart from the top surface, the third bottom surfaces lying below the second bottom surfaces

~~forming a layer of conductive material on the layer of insulation material to fill up the second trench and the first trenches; and~~

~~planarizing the layer of conductive material to form a trace~~.

15. (Currently Amended) The method of claim 14 wherein the second etching step includes the steps of:

forming a layer of masking material on the layer of insulation material;

patterning the layer of masking material to expose a portion of the top surface of the layer of insulation material and the plurality of first trenches; and

anisotropically etching the layer of ~~masking~~ insulation material and the plurality of first trenches to form the second trench.

16. (Currently Amended) The method of claim 14 ~~wherein the trace is formed to have a number of loops~~ and further comprising the steps of:

forming a layer of conductive material on the layer of insulation material to fill up the second trench; and

planarizing the layer of conductive material to form a conductive region, the conductive region having a top surface that is substantially planar with the top surface of the layer of insulation material.

17. (Currently Amended) The method of claim ~~15~~ 16 wherein ~~the loops~~ the conductive region is formed to have a number of loops that lie substantially in a same plane.

18. (Currently Amended) The method of claim ~~14~~ 16 wherein the ~~trace~~ conductive region is connected to a contact.

19. (Currently Amended) The method of claim ~~14~~ 16 wherein the ~~trace~~ conductive region is connected to a via.

20. (Currently Amended) The method of claim ~~14~~ 16 wherein the layer of conductive material includes:

a layer of barrier material formed on the layer of insulation material;

a layer of seed material formed on the layer of barrier material; and

a layer of copper formed on the layer of seed material.

21. (New) A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a top surface; and

etching the layer of insulation material to form a first trench in the layer of insulation material, the first trench having a first bottom surface vertically spaced a first distance apart from the top surface.

22. (New) The method of claim 21 and further comprising the step of etching the layer of insulation material and the first trench to form a second trench in the layer of insulation material, the second trench having a second bottom surface vertically spaced a second distance apart from the top surface, and a third bottom surface vertically spaced a third distance apart from the top surface, the third bottom surface lying below the second bottom surface.

23. (New) The method of claim 22 and further comprising the steps of:

forming a layer of conductive material on the layer of insulation material to fill up the second trench; and

planarizing the layer of conductive material to form a conductive region, the conductive region having a top surface that is substantially planar with the top surface of the layer of insulation material.

24. (New) The method of claim 23 wherein the second etching step includes the steps of:

forming a layer of masking material on the layer of insulation material;

patterning the layer of masking material to expose the first trench and a portion of the top surface of the layer of insulation material;

anisotropically etching the layer of insulation material and the first trench to form the second trench.

25. (New) The method of claim 23 wherein the conductive region is formed to have a number of loops.

26. (New) The method of claim 25 wherein the loops lie substantially in a same plane.

27. (New) The method of claim 23 wherein the conductive region is connected to a contact.

28. (New) The method of claim 23 wherein the conductive region is connected to a via.

29. (New) The method of claim 23 wherein the layer of conductive material includes:

a layer of barrier material formed on the layer of insulation material;

a layer of seed material formed on the layer of barrier material; and

a layer of copper formed on the layer of seed material.